REMARKS

In accordance with the foregoing, claims 1, 4, 11, 20, 23, 29 and 36 have been amended. No new matter has been added. Claims 1-4, 6-11, 13-23, 25-29, and 31-36 are pending and under consideration.

Rejections under 35 U.S.C. §103(a)

The Office Action rejects claims 11, 13-17, 19, 29, and 31-36 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,915,025 issued to Taguchi et al. (hereinafter referred to as "Taguchi"), and further in view of U.S. Patent No. 4,525,599 issued to Curran et al. (hereinafter referred to as "Curran"), and further in view of Schneier (Applied Cryptography: Second Edition). In addition, the Office Action rejects claims 1-3, 6-10, 21-22, and 25-28 under 35 U.S.C. §103 (a) as being unpatentable over the combination of Taguchi, Curran and Schneier and further in view of U.S. Patent No. 5,706,445 issued to Milhaupt et al. (hereinafter referred to as "Milhaupt"). Finally, the Office Action rejects claims 4 and 23 under 35 U.S.C. §103(a) as being unpatentable over the combination of Taguchi, Curran and Schneier and further in view of IBM Technical Disclosure Bulletin 19800601 (hereinafter referred as "IBM"). These rejection are all respectfully traversed.

Claim 11 recites:

> said internal circuit has information rewrite means for ciphering and rewriting at least part of the information stored in said external memory in a predetermined initialization operation ... and **said predetermined initialization operation is executed when the apparatus is first powered on**

(emphasis added) in the last paragraph. As acknowledged in the Office Action, page 6, lines 6-8, Taguchi does not specifically disclose that the initialization operation is an initialization operation when the apparatus is powered on. Regarding this feature, the Office Action states in page 7, line 20 – page 8, line 2, that "it would have been obvious to have the device programmed/configured with the key updating routine and re-encryption routines prior to the devices being first powered on. This would have been obvious because the ordinary person skilled in the art would have been motivated to prevent needing to update the device to provide this functionality to the device at a later time." However, as previously argued, Taguchi merely teaches "[u]sing the time management table 59, the time management means manages the life of each of the keys used and the time that has elapsed since the key in question was last updated" in column 14, fines 58-61, which is nothing to do with a "predetermined initialization operation executed when the apparatus is first powered

on" as recited in claim 11. None of Taguchi and the remaining prior art of record teaches or suggests this feature of claim 11 as well as any motivation to modify Taguchi to have this feature of claim 11. Therefore, the rationale for obviousness rejection here in the Office Action appears to be common knowledge (well-known), but there is no evidence supporting the Examiner's assertion (see M.P.E.P. §2144.03(B) ("there must be some form of evidence in the record to support an assertion of common knowledge"). The applicants respectfully request that the Examiner provide such an evidence that shows "the internal circuit has information rewrite means for ciphering and rewriting at least part of the information stored in said external memory **in a predetermined initialization operation executed when the apparatus is first powered on**" as recited in claim 11. At least for this reason, claim 11 as well as claims 13-17 and 19, which depend therefrom, are patentably distinguishable over Taguchi, Curran and Schneier. Accordingly, withdrawal of the rejections over these claims is requested. Claims 29 and 36 recite similar features as those of claim 11. Thus, claims 29 and 36 as well as claims 31-35, which depend from claim 29, are also patentably distinguishable over the cited references for the same reasons described above for claim 11. Accordingly, withdrawal of the rejections over these claims is requested.

Claim 1 recites:

> said internal circuit further comprises a ciphering section interposed at an entrance to an external side of said internal circuit ... said ciphering section is supplied with a second clock and performs ciphering synchronously with the supplied second clock and a clock supply section for supplying **the second clock at a higher speed than a speed of the first clock supplied to said CPU, to said ciphering section, so that the ciphering patterns vary depending on clock speed**

(emphasis added) in the last paragraph. According to claim 1, the ciphering section is supplied with the second clock faster than the first clock supplied to the CPU so that the ciphering patterns can vary depending on clock speed. This amendment is supported in the specification, for example, in page 23, line 14 to page 24, line 7. None of the prior art of record teaches or suggests more than one clock operating within a internal circuit and further, the first clock supplied to the CPU and the second clock supplied to the ciphering section of different speeds to vary the ciphering patterns. Therefore, claim 1 as well as claims 2-4, 6-10 and claim 18, which depend therefrom, are patentably distinguishable over Taguchi, Curran, Schneier, IBM and Milhaupt because the combinations thereof relied on in the Office Action fail to teach or suggest "**said internal circuit further comprises a ciphering section supplied with a second clock at a higher speed than a speed of the first clock supplied to**

the CPU so that the ciphering patterns vary depending on clock speed" as recited in claim 1. Accordingly, withdrawal of the rejections over these claims is requested. Claim 20 recites similar features as those of claim 1. Thus, claim 20 as well as claims 21-23 and 25-28, which depend therefrom, are also patentably distinguishable over the cited references for the same reasons described above for claim 1.

Claims 4 and 23 are also patentable based on the features recited therein. Claims 4 and 23 now recite "**the ciphering section of the internal circuit further comprises a bus interface that externally outputs data ciphered by the ciphering section when access to the external device is requested and externally outputs dummy data when access to the external device is not requested**". This amendment is supported in the specification, for example, page 20, lines 11-21. The purpose of transmitting the dummy data is to make illicit interpretation more difficult (see the specification, page 4, line 15). The features recited in claims 4 and 23 and what is described in IBM are totally different in terms of purpose. Because the purpose of IBM is different from that of claims 4 and 23, IBM fails to disclose or suggest that dummy data is output when there is no request for access to the external device as recited in claims 4 and 23. IBM aims to check whether access is possible or not and thus, it inevitably needs to try access to a generated random address. Therefore, claims 4 and 23 are also patentably distinguishable over the cited references based on the features recited therein in addition to the dependencies upon claims 1 and 20, respectively.

Summary

Claims 1-4, 6-11, 13-23, 26-29, and 31-36 are pending and under consideration. It is respectfully submitted that none of the references taken alone or in combination disclose the present claimed invention.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,
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